DHA®

QJ/DHA 01.56-2018

# LD4263

## Automotive 5V Low Drop Voltage Regulator IC

### Description

LD4263 is a 5-V low drop voltage regulator. The maximum input voltage is 45 V. The maximum output current is more than 200 mA. The IC is short-circuit proof and incorporates temperature protection which turns off the IC at over temperature.

The IC regulates an input voltage $V_I$ in the range of 6V < $V_I$ < 45V to $V_Q$,nom = 5.0V. A reset signal is generated for an output voltage of $V_Q$,rt < 4.5V. This voltage threshold can be decreased to 3.5V by external connection of a voltage divider. The reset delay can be set externally by a capacitor. The integrated watchdog logic supervises the connected microcontroller. The IC can be switched off via the inhibit input, which causes the current consumption to drop from 900 μ A to typical 0 μ A.

### Features

- Output voltage tolerance ⩽±2%
- 200 mA output current capability
- Low-drop voltage
- Very low standby current consumption
- Overtemperature protection
- Reverse polarity protection
- Short-circuit proof
- Adjustable reset threshold
- Watchdog
- Wide temperature range
- Suitable for use in automotive electronics

### Ordering Information

| Package | Remarks |
|---|---|
| SOP8 | Tubed, Reeled, Pb-free |
| SOP14 | Tubed, Reeled, Pb-free |
| SOP20W | Tubed, Reeled, Pb-free |

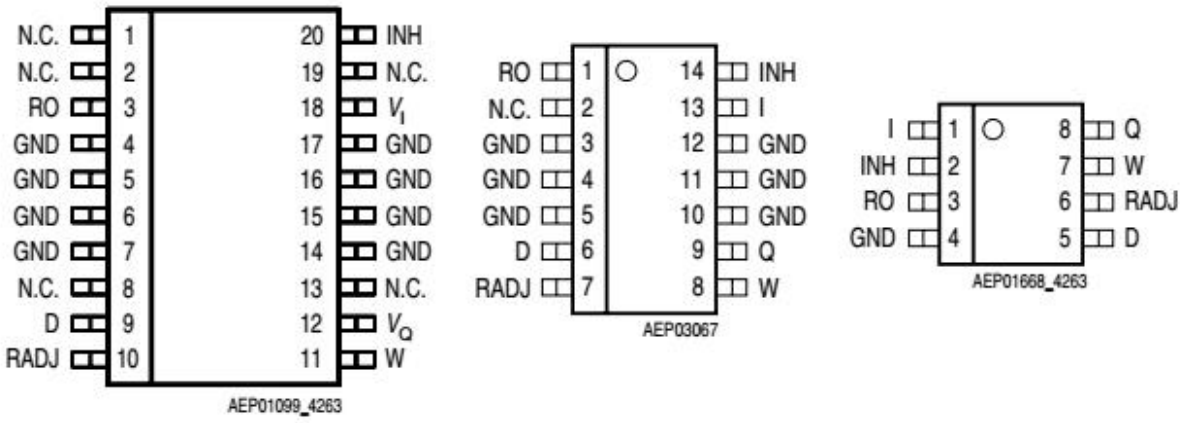



**Figure 1. Pins Figure**

## Pin Description

| Symbol | Fuaction |
|---|---|
| I | **Input**. The input voltage is applied to the IC. Use the ceramic capacitor connected between this pin and the ground. |
| INH | **Inhibit input**. TTL-compatible, low-active voltage. |
| RO | **Reset and watchdog output**. Open-collector out-put connected to the output via resistor of 30 kΩ. |
| GND | **Ground** |
| D | **Reset delay**. The capacitor is connected between this output and the ground to adjust the delay time. |
| RADJ | **Reset threshold**. For setting the switching thresh-old, connect a voltage divider (from output Q $V_Q$ to ground) to the pin. If this input is connected to ground, the reset is triggered at the internal thresh-old. |
| W | **Watchdog input**. Positive-edge-triggered input at least 5 V/μs for monitoring a microcontroller. |
| Q | **Output**. Connected to the ground via an external tantalum capacitor with a minimum capacity of 22 μF and 1 Ω ≤ ESR ≤ 3 Ω within the operating temperature range at frequency of 10 kHz |

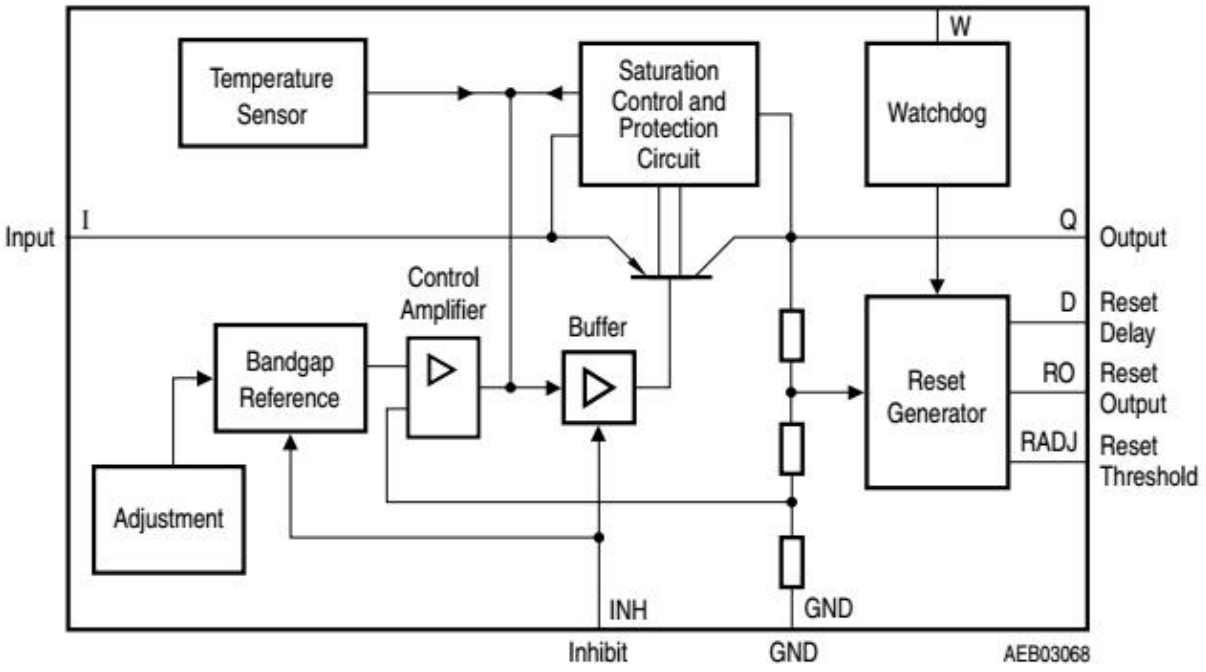



**Figure 2. Block Diagram**

## Absolute Maximum Ratings

| Parameters | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Input voltage | $U_I$ | -42 | 45 | V |
| Output voltage on output reset | $U_R$ | -0.3 | 42 | V |
| Voltage on reset adjust input | $U_{RADJ}$ | -0.3 | 6 | V |
| Voltage on reset delay pin | $U_D$ | -0.3 | 42 | V |
| Output voltage | $U_Q$ | -0.3 | 7 | V |
| Inhibit input voltage | $U_{INH}$ | -42 | 45 | V |
| Input watchdog voltage | $U_W$ | -0.3 | 6 | V |
| Junction temperature | $T_J$ | -40 | 150 | ℃ |

## Electrical parameters

$V_I$ =13.5 V， $V_{INH}$ > 3.5V， Tamb = 25℃， −40℃<$T_J$ <1 25℃，（unless specified otherwise）

| Parameters | Test condition | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Normal Operation** | | | | | | |
| Output voltage | 5mA≤$I_Q$≤150mA, 6V≤$V_I$≤28V | $V_Q$ | 4.9 | 5.0 | 5.1 | V |
| | $I_Q$=100mA, 6V≤$V_I$≤32V | | 4.9 | 5.0 | 5.1 | |
| | $I_Q$=5mA, $V_I$=45V | | 4.8 | 5.0 | 5.2 | |
| Output current | | $I_Q$ | 200 | 250 | 400 | mA |
| Current consumption Iq = $I_I$ -$I_Q$ | $V_{INH}$ = 0V | Iq | | 0 | 0.05 | mA |
| | $I_Q$ =0mA | | | 0.9 | 1.3 | |
| | $I_Q$ =150mA | | | 10 | 18 | |
| | $I_Q$ =150mA, UI =4.5V | | | 15 | 23 | |
| Drop voltage | $I_Q$ =150mA | Vdr | | 0.35 | 0.5 | V |
| Line regulation | $I_Q$=150mA, $V_I$= 6V to 28V | $\Delta U_{Q(U)}$ | | 3 | 25 | mV |
| Load regulation | $I_Q$=5mA to 150mA | $\Delta U_{Q(I)}$ | | | 25 | mV |

| Parameters | Test condition | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Reset Generator** | | | | | | |
| Switching threshold | $U_{RADJ}$ =0V, $I_Q$ =5mA | $U_{RT}$ | 4.5 | 4.65 | 4.8 | V |
| Reset adjust threshold | $I_Q$ =5mA | $U_{RADJTH}$ | 1.26 | 1.35 | 1.44 | V |
| Reset low voltage | R1 = 5.6kΩ , $I_{RO}$=1mA | $U_{ROL}$ | | 0.1 | 0.4 | V |
| Saturation voltage | R1 = 5.6kΩ | $U_{Dsat}$ | | 50 | 100 | mV |
| Upper timing threshold | $I_Q$ =5mA | $U_{DU}$ | 1.45 | 1.70 | 2.05 | V |
| Lower reset threshold | $I_Q$ =5mA | $V_{DRL}$ | 0.20 | 0.35 | 0.55 | V |
| Charge current | $I_Q$ =5mA | $I_{D,ch}$ | 40 | 60 | 85 | μA |
| Reset delay time | $I_Q$ =5mA, C1 =100nF | $t_{RD}$ | 1.3 | 2.8 | 4.1 | ms |
| **Watchdog** | | | | | | |
| Discharge current | $I_Q$ =5mA, $U_D$ =1.0V | $I_{D,wd}$ | 4.40 | 6.25 | 9.10 | μA |
| Watchdog trigger time | $I_Q$ =5mA, C1 =100nF | $t_{WI,tr}$ | 16 | 22.5 | 27 | ms |
| **Inhibit** | | | | | | |
| Switching voltage | IC turned on | $V_{INH,ON}$ | 3.6 | | | V |
| Turn-OFF voltage | IC turned off | $V_{INH,OFF}$ | | | 0.8 | V |
| Input current | $V_{INH}$ = 5V | $I_{INH}$ | 5 | 10 | 25 | μA |

## Circuit Description

The error amplifier compares the reference voltage which is maintained with high precision resistor adjustment with a voltage that is proportional to the output voltage, and drive the serial transistor through the buffer. Saturation control, depending on the load current, prevents any powerful element over saturation. If externally scaled output voltage at the input reset threshold RADJ falls below 1.35 V (typical valuation), then external delay reset discharge by the reset generator. When the capacitor voltage reaches lower threshold $U_{DRL}$, at the out-put the reset signal appears and held as long as the upper limit $U_{DU}$ exceeded. If the reset threshold input RADJ is connected to GND, then the reset is triggered at the output voltage of 4.65 V (typical valuation). The connected micro controller operation is monitored by Watchdog function. In the absence of pulses on pin W, RO reset output is set to a low level. Reset delay time can be set in a wide range by the reset delay capacitor. The IC can be switched on the inhibit input with active low level. The IC also contains a number of internal circuits for over-load and over temperature protection, reverse polarity protection.

## Reset Timing

Power-up reset delay time is determined by the charge time of the external delay capacitor $C_D$, nF, that can be calculated as follows

$$C_D = (t_{rd} \times I_{D,ch}) / U$$

where trd – reset delay time, ns,

$I_{D,ch}$ – charging current, µA (typical value 60 µA),

$U = U_{DU}$ – threshold RO output switching voltage to a high voltage state, V (typical value is 1.7 V).

## Reset switching threshold

On default, installed typical value of reset switching threshold is 4.65 V. Using the LD4263 the reset threshold can be set to 3.5 V < $U_{RT}$ < 4.6 V by connection to RADJ external resistive divider. Calculation is performed simplified as a reset input current adjustment may be neglected. If this function is not required, the RADJ pin should be connected to GND. The threshold voltage of output reset generator $U_{RT}$, V, is calculated by formula

$$U_{RT} = (1 + R1 / R2) \times U_{RADJTH},$$

where $U_{RADJTH}$ – switching threshold voltage at the input reset adjustment ,V (typical value 1.35 V).

## Timing of the Watchdog function

Watchdog pulse frequency should be higher than the frequency of the minimum pulse sequence that is determined by the external reset delay capacitor $C_D$. Timing calculation $t_{WI,tr}$, ms is carried out according to the formula

$$t_{WI,tr} = ((U_{DU} - U_{DWL}) / I_{D,wd}) \times C_D,$$

where $U_{DWL}$ – threshold voltage of the reset switch outputs to a low state,

V, $I_D$, wd – discharge current, uA.

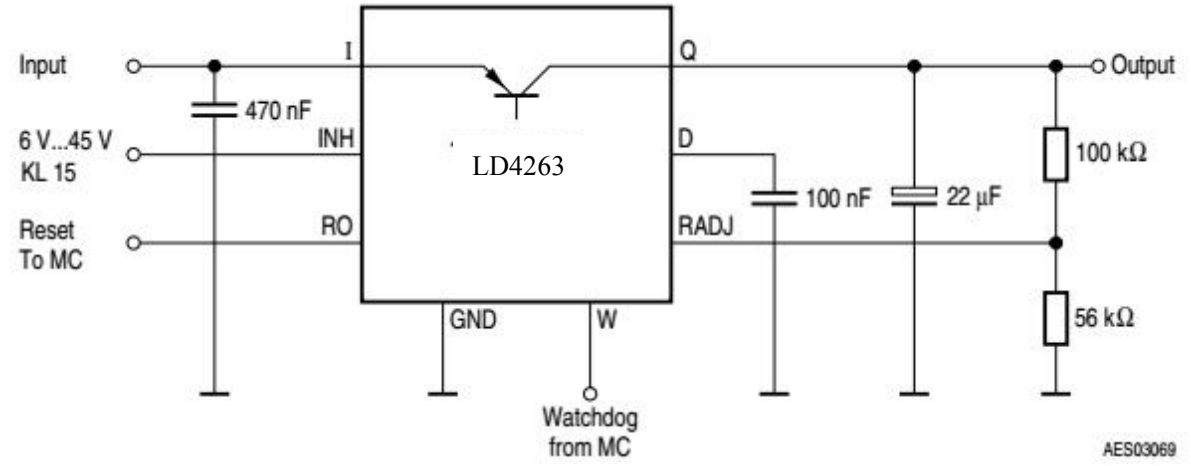



**Figure 3. Typical application circuit diagram**

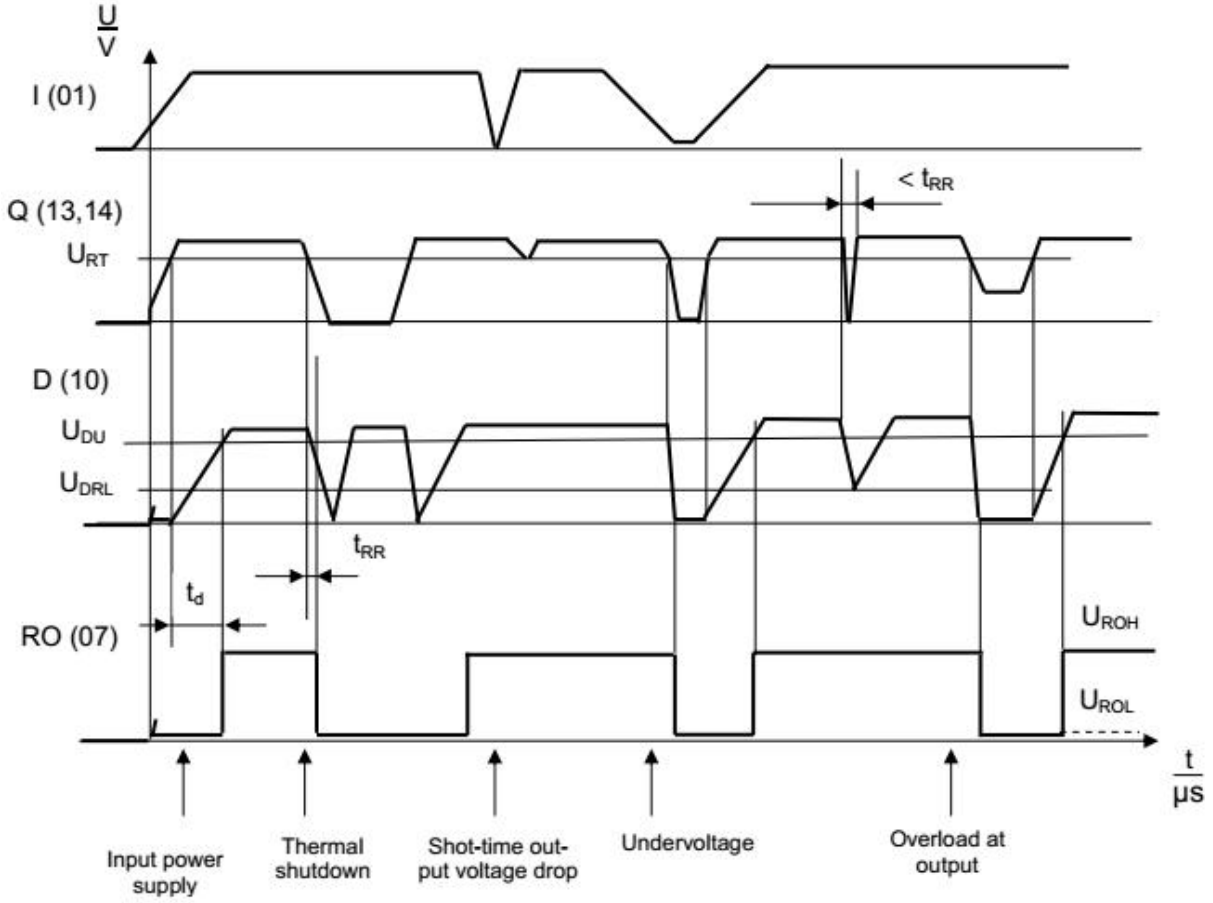



**Figure 4. Timing diagram (the Watchdog function is not active)**

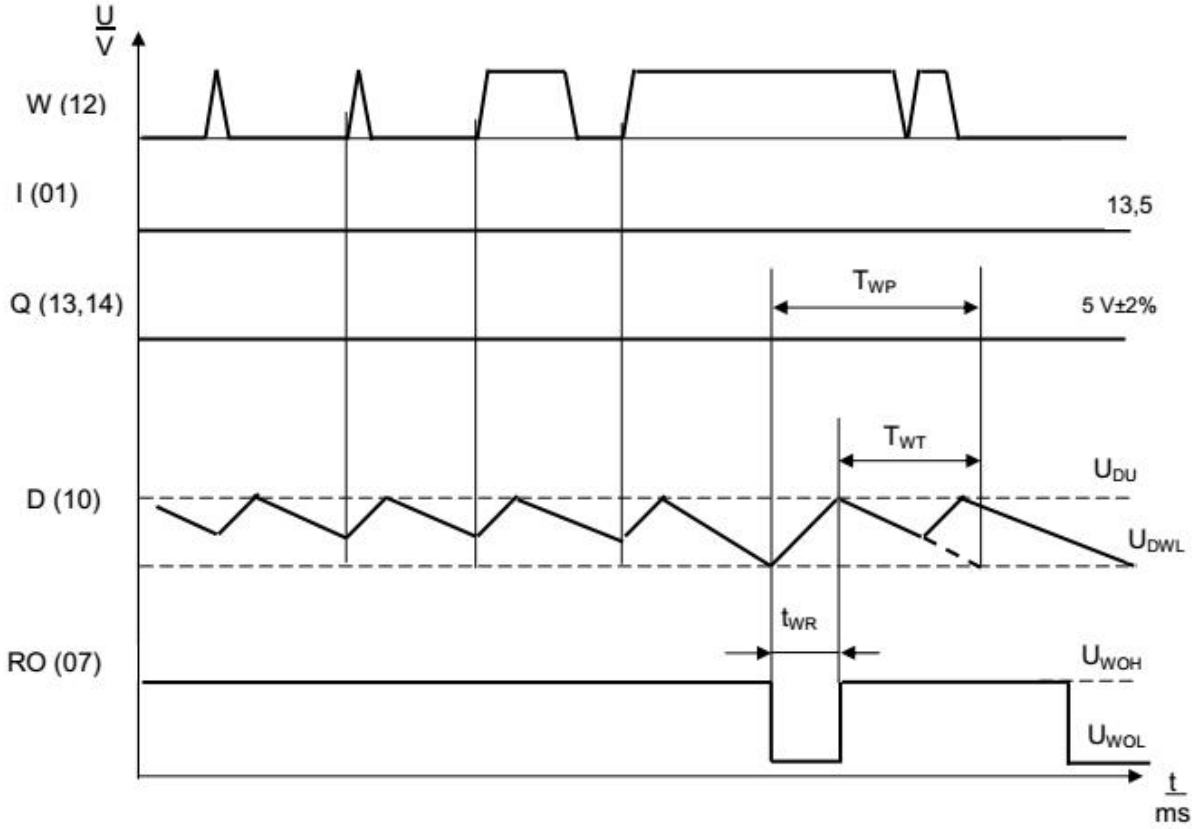
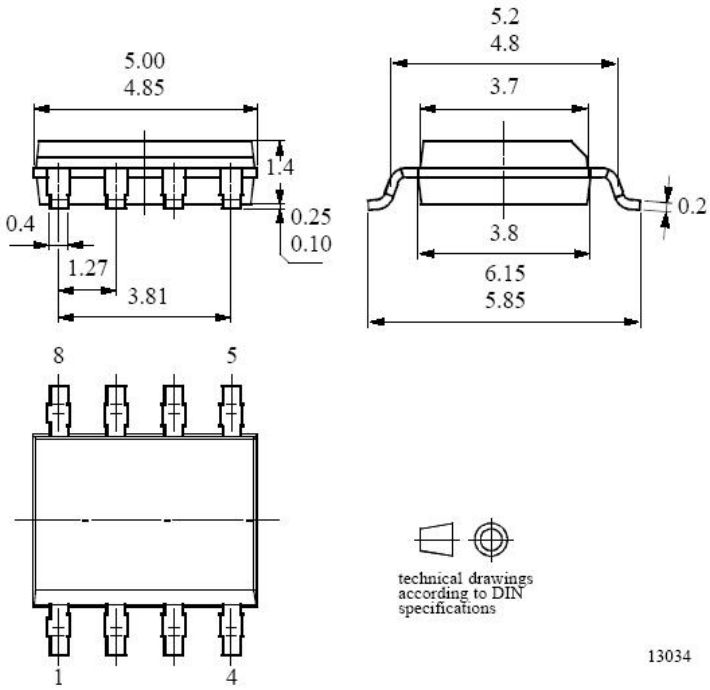



**Figure 5. Timing diagram of the active Watchdog function**

## Package Information

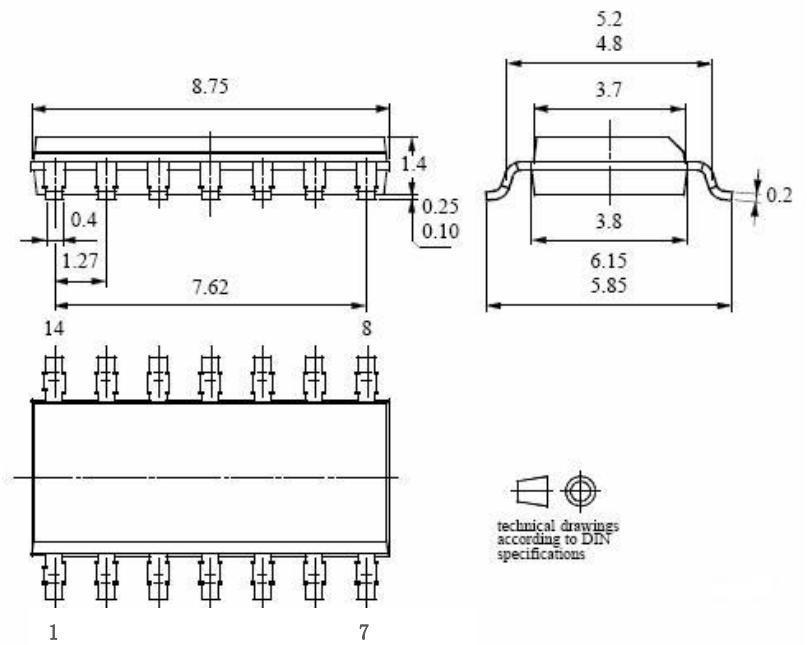
### SOP8

Dimensions in mm




### SOP14

Dimensions in mm



**SOP20W**
Dimensions in mm