5V Low Drop Voltage Regulator IC

Description

The LD4275(TLE4275) is a monolithic integrated low-drop voltage regulator in a 5 pin TO-package. An input voltage up to 45 V is regulated to $V_{Q,nom}$ = 5.0 V. The IC is able to drive loads up to 450 mA and is short-circuit proof. At over temperature the LD4275 is turned off by the incorporated temperature protection. A reset signal is generated for an output voltage $V_{Q,rt}$ of typ. 4.65 V. The delay time can be programmed by the.external delay capacitor.

Features

- Output voltage 5 V ± 2%
- Very low current consumption
- Power-on and undervoltage reset
- Reset low down to VQ = 1 V
- Very low-drop voltage
- Short-circuit-proof
- Reverse polarity proof
- Suitable for use in automotive electronics
- ESD protection > 4 kV

Dimensioning Information on External Components

The input capacitor CI is necessary for compensation of line influences. Using a resistor of approx. 1Ω in series with C_I, the oscillating of input inductivity and input capacitance can be damped. The output capacitor C_Q is necessary for the stability of the regulation circuit. Stability is guaranteed at values C_Q ⩾ 22 µF and an ESR of ⩽ 5Ω within the operating temperature range.

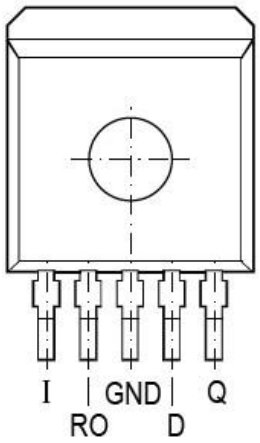
Circuit Description

The control amplifier compares a reference voltage to a voltage that is proportional to the output voltage and drives the base of the series transistor via a buffer. Saturation control as a function of the load current prevents any over saturation of the power element. The IC also incorporates a number of internal circuits for protection against:

- Overload
- Over-temperature
- Reverse polarity

Pin Description

Pin	Symbol	Function
1	I	**Input**; block to ground directly at the IC by a ceramic capacitor.
2	RO	**Reset Output**; open collector output
3	GND	**Ground**; Pin 3 internally connected to heat sink
4	D	**Reset Delay**; connect capacitor to GND for setting delay time
5	Q	**Output**; block to ground with a ≥ 22 µF capacitor, ESR < 5 Ω at 10 kHz.



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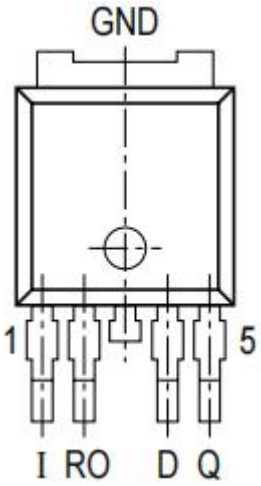

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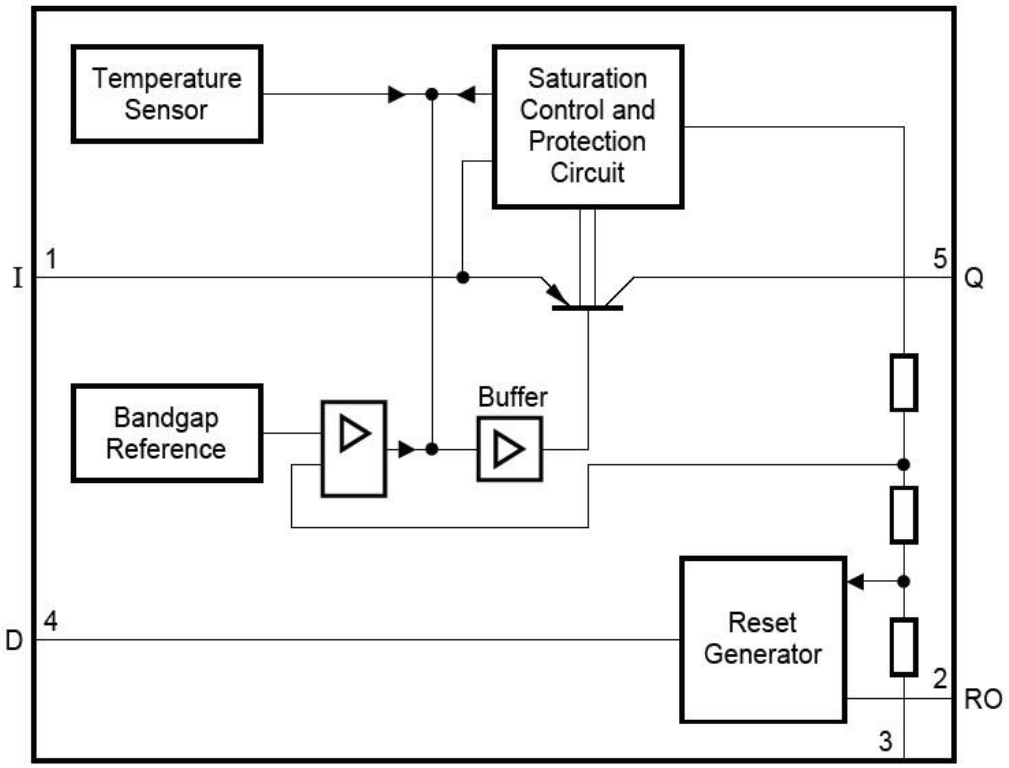
Block Diagram



Electrical Characteristics

V_I = 13.5 V; – 40℃ < Tj < 150 ℃ (unless otherwise specified)

Parameters	Test Conditions / Pins	Symbol	Min	Typ	Max	Unit
Output voltage	5 mA < I_Q < 400mA 6 V < V_I < 28 V	V_Q	4.9	5.0	5.1	V
Output voltage	5 mA < I_Q < 200mA 6 V < V_I < 40 V	V_Q	4.9	5.0	5.1	V
Output current limitation		I_Q	450	700		mA
Current consumption Iq = I_I – I_Q	I_Q = 1 mA; Tj = 25℃	Iq		150	200	μA
Current consumption Iq = I_I – I_Q	I_Q = 1 mA; Tj = 85℃	Iq		150	220	μA
Current consumption Iq = I_I – I_Q	I_Q = 150 mA	Iq		5	10	μA
Current consumption Iq = I_I – I_Q	I_Q = 400 mA	Iq		12	22	μA
Drop voltage[1])	I_Q =300mA Vdr = V_I – V_Q	Vdr		250	500	mV
Load regulation	I_Q = 5 mA to 400 mA	ΔV_Q		15	30	mV
Line regulation	ΔV_I =8 V to 32 V I_Q = 5 mA	ΔV_Q	-15	5	15	mV
Power supply ripple rejection	fr = 100 Hz; Vr = 0.5 Vpp	PSRR		60		dB
Temperature output voltage drift		dV_Q/dT		0.5		mV/K
Reset switching threshold		$V_{Q,rt}$	4.5	4.65	4.8	V
Reset output low voltage	Rext ≥ 5 kΩ; V_Q > 1 V	V_{ROL}		0.2	0.4	V
Reset output leakage current	V_{ROH} = 5 V	I_{ROH}		0	10	μA
Reset charging current	V_D = 1 V	$I_{D,c}$	3.0	5.5	9.0	μA
Upper timing threshold		V_{DU}	1.5	1.8	2.2	V
Lower timing threshold		V_{DRL}	0.2	0.4	0.7	V
Reset delay time	C_D = 47 nF	trd	10	16	22	ms
Reset reaction time	C_D = 47 nF	trr		0.5	2	μs

Maximum Ratings

Symbol	Parameter	Limit Values		Test Condition
		Min	Max	
V_I	Input Voltage	-42V	45V	
I_I	Input Current	-	-	Internally limited
V_Q	Output Voltage	-10V	16V	
I_Q	Output Current	-	-	Internally limited
V_{RO}	Reset Output Voltage	-0.3V	25V	
I_{RO}	Reset Output Current	-5mA	5mA	
V_D	Reset Delay Voltage	-03V	7V	
P_D	Reset Delay Current	-2mA	2mA	
Tj	Junction temperature	-40℃	150℃	
Tstg	Storage temperature	-50℃	150℃	
Note: Maximum ratings are absolute ratings; exceeding any one of these values may cause irreversible damage to the integrated circuit.				

Application Diagram