PWM Power Controller IC

Description

The LD6083B (analog U6083B) is a PWM IC in bipolar technology for the control of an N-channel power MOSFET used as a high side switch. The IC is ideal for use in the brightness control (dimming) of lamps e.g., in dashboard applications.

Features

- Pulse-width modulation up to 2 kHz clock frequency
- Protection against short circuit, load dump, overvoltage and reverse V_S
- Duty cycle 18 to 100% continuously
- Internally reduced pulse slope of lamp's voltage
- Charge pump noise suppressed
- Ground wire breakage protection
- Interference and damage protection according to VDE 0839 and ISO/TR 7637/1

Ordering Information

Package	Remarks
SOP8	Tubed, Reeled, Pb-free
DIP8	Tubed, Pb-free

Block Diagram

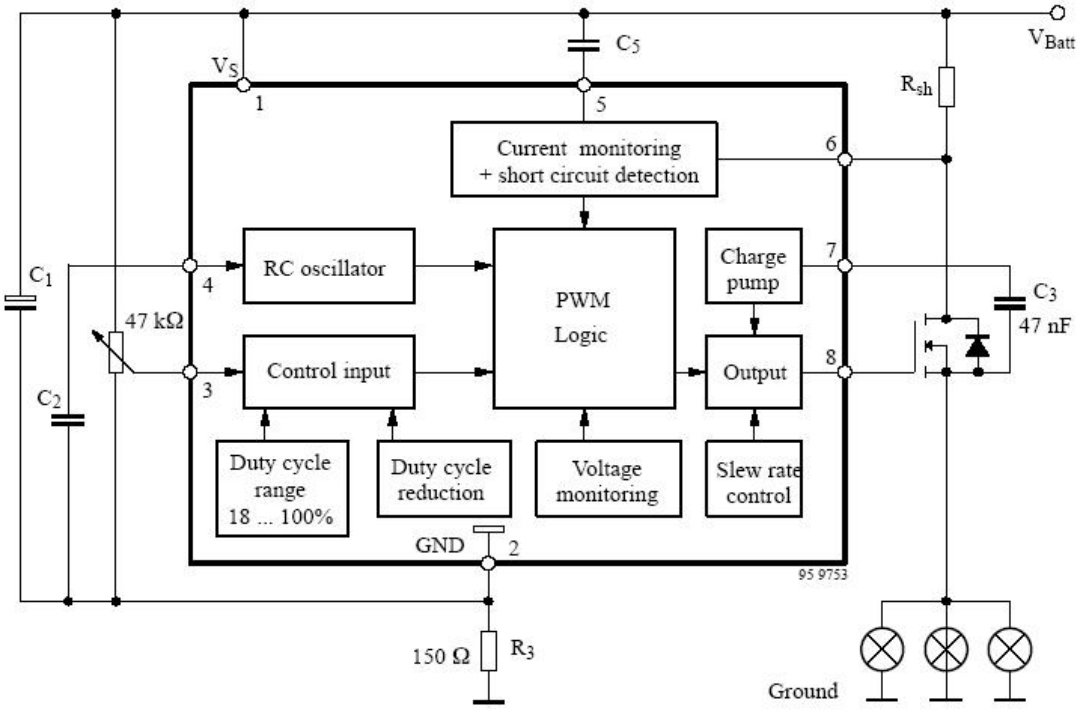
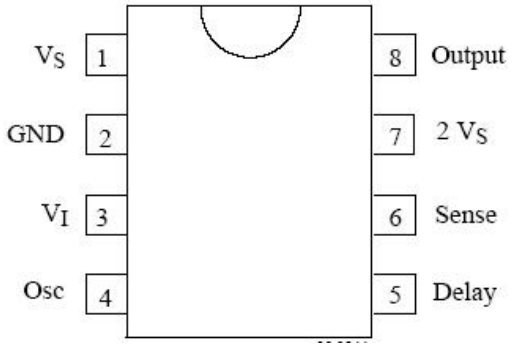


Figure 1. Block diagram with external circuit

Pin Description



Pin	Symbol	Function
1	V_S	Supply voltage VS
2	GND	IC ground
3	V_I	Control input (duty cycle)
4	Osc	Oscillator
5	Delay	Short circuit protection delay
6	Sense	Current sensing
7	$2V_S$	Voltage double
8	Output	Output

Functional Description

Pin 1, Supply Voltage, V_S or V_{Batt}

Overvoltage Detection

Stage 1: If overvoltage V_{Batt} > 20 V (typ.) occur, the external transistor is switched off and switched on again at V_{Batt} < 18.5 V (hysteresis).

Stage 2: If V_{Batt} > 28.5 V (typ), the voltage limitation of the IC is reduced from V_S = 26 V to 20 V. The gate of the external transistor remains at the potential of the IC ground, thus producing voltage sharing between FET and lamps in the event of overvoltage pulses occuring (e.g., load dump).

The short-circuit protection is not in operation. At V_{Batt} approx. < 23 V, the overvoltage detection stage 2 is switched off. Thus during overvoltage detection stage 2 the lamp voltage V_{Lamp} is calculated to :

$V_{Lamp} = V_{Batt} - V_S - V_{GS}$

V_S = Supply voltage of the IC at overvoltage detection stage 2

VGS = Gate – source voltage of the FET

Undervoltage Detection

In the event of voltages of approximately V_{Batt} < 5.0 V, the external FET is switched off and the latch for short circuit detection is reset.

A hysteresis ensures that the FET is switched on again at approximately V_{Batt} ⩾5.4 V.

Pin 2, GND

Ground-Wire Breakage

To protect the FET in the case of ground-wire breakage, a 1MΩ resistor between gate and source it is recommended to provide proper switch-off conditions.

Pin 3, Control Input

The pulse width is controlled by means of an external potentiometer (47kΩ). The characteristic (angle of rotation/duty cycle) is linear. The duty cycle can be varied from 18 to 100%. It is possible to further restrict the duty cycle with the resistors R1 and R2 (see figure 3).

In order to reduce the power dissipation of the FET and to increase the lifetime of the lamps, the IC automatically reduces the maximum duty cycle at Pin 8 if the supply voltage exceeds V2 = 13 V. Pin 3 is protected against short-circuit to V_{Batt} and ground (V_{Batt} ≤16.5 V).

Pin 4, Oscillator

The oscillator determines the frequency of the output voltage. This is defined by an external capacitor,C_2. It is charged with a constant current, I, until the upper switching threshold is reached. A second current source is then activated which taps a double current, 2×I, from the charging current. The capacitor, C_2, is thus discharged at the current, I, until the lower switching threshold is reached. The second source is then switched off again and the procedure starts once more.

Example for Oscillator Frequency Calculation:

Switching thresholds

V_{T100} = High switching threshold (100% duty cycle)

$V_{T100} = V_S \times \alpha_1 = (V_{Batt} - I_S \times R_3) \times \alpha_1$

$V_{T<100}$ = High switching threshold (< 100% duty cycle)

$V_{T<100} = V_S \times \alpha_2 = (V_{Batt} - I_S \times R_3) \times \alpha_2$

V_{TL} = Low switching threshold

$V_{TL} = V_S \times \alpha_3 = (V_{Batt} - I_S \times R_3) \times \alpha_3$

whereas

α_1, α_2 and α_3 are fixed constant.

Calculation Example

The above mentioned threshold voltages are calculated for the following values given in the data sheet.

V_{Batt} = 12 V, I_S = 4 mA, R_3 = 150 Ω, α_1 = 0.7, α_2 = 0.67 and α_3 = 0.28.

$V_{T100} = (12\ V - 4\ mA \times 150\Omega) \times 0.7 \approx 8\ V$

$V_{T<100}$ = 11.4 V × 0.67 = 7.6 V

V_{TL} = 11.4 V × 0.28 = 3.2 V

Oscillator Frequency

3 cases have to be distinguished

1) f_1 for duty cycle = 100%, no slope reduction with capacitor C_4 (see figure 3)

$$f_1 = \frac{I_{osc}}{2 \times (V_{T100} - V_{TL}) \times C_2}$$, whereas C_2= 68 nF, I_{osc} = 45 µA, f_1 = ... = 75 Hz

2) f_2 for duty cycle < 100%, no slope reduction with capacitor C_4

For a duty cycle of less than 100%, the oscillator frequency, f, is as follows:

$$f_2 = \frac{I_{osc}}{2 \times (V_{T<100} - V_{TL}) \times C_2}$$, whereas C_2 = 68 nF, I_{osc} = 45 µA, f_2 = ... = 69 Hz

3) f_3 with duty cycle < 100% with slope reduction capacitor C_4 (see page 3 “Output Slope Control”)

$$f_3 = \frac{I_{osc}}{2 \times (V_{T<100} - V_{TL}) \times C_2 + 2V_{Batt} \times C_4}$$

whereas C_2= 68 nF, C_4 = 1.8 nF, I_{osc} = 45 µA, f_3 = ... = 70 Hz

By selecting different values of C_2 and C_4, it is possible to have a range of oscillator frequency, f, from 10 to 2000 Hz as shown in the data sheet.

Output Slope Control

The slope of the lamp voltage is internally limited to reduce radio interference, by limitation of the voltage gain of the PWM comparator.

Thus the voltage rise on the lamp is proportional to the oscillator voltage increase at the switchover time according to the equation.

$dV_8/dt = \alpha_4 \times dV_4/dt = 2 \times \alpha_4 \times f \times (\alpha_2 - \alpha_3) \times (V_{Batt} - I_S \times R_3)$

when f = 75 Hz, $V_{TX} = V_{T<100}$ and $\alpha_4 = 63$

we obtain

$dV_8/dt = 2 \times 63 \times 75\ Hz \times (0.67–0.28) \times (12\ V - 4\ mA \times 15\Omega) = 42\ V/ms$

Via an external capacitor, C_4, the slope can be further reduced as follows:

$dV_8/dt = I_{OSC} / (C_4 + C_2/\alpha_4)$

when I_{OSC} = 45 µA, C_4 = 1.8 nF, C_2 = 68 nF and $\alpha_4 = 63$

then dV_8/dt = 45 µA/ (1.8 nF + 68 nF/63) = 15.6 V/ms

To damp oscillation tendencies, a resistance of 100 Ω in series with capacitance C_4 is recommended.

Interference Suppression

"On board" radio reception according to VDE 0879 part 3/4.81

Test conditions refering to figure 2.

Application circuit according to figure 1 or 3.

Load: nine 4-W lamps in parallel.

Duty cycle = 18%, V_{Batt} = 12 V, f_{OSC}= 100 Hz

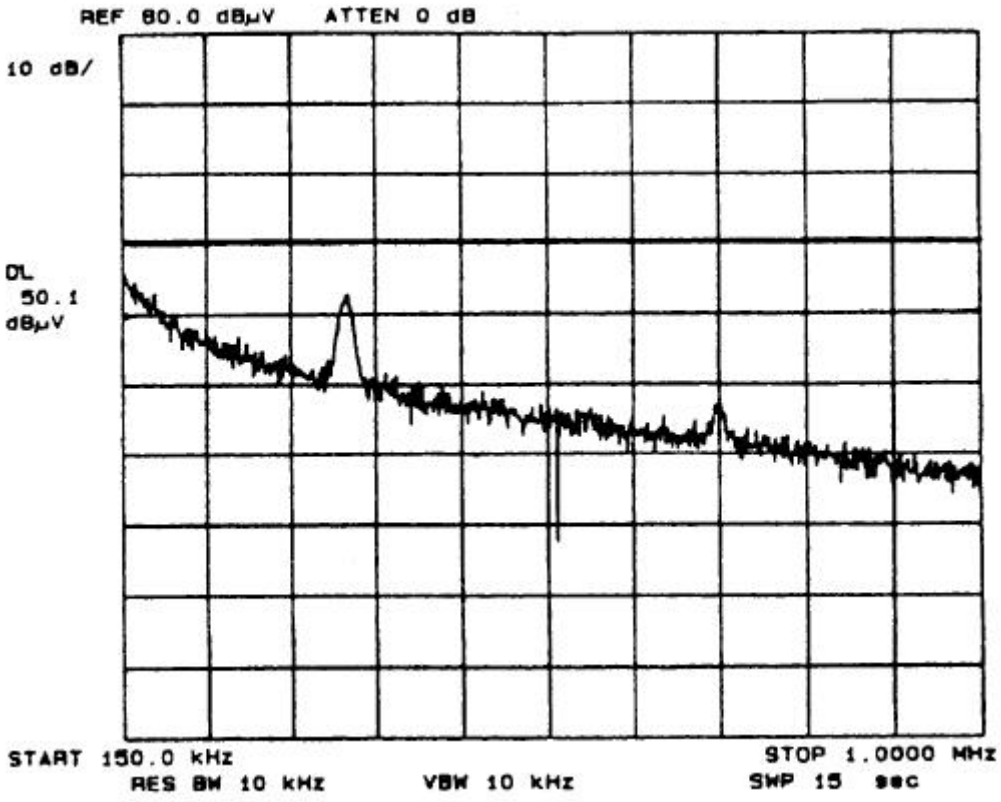


Figure 2. Voltage spectrum of on-board radio reception

Pins 5 and 6, Short-Circuit Protection and Current Sensing,

1. Short-Circuit Detection and Time Delay, td

The lamp current is monitored by means of an external shunt resistor. If the lamp current exceeds the threshold for the short-circuit detection circuit (V_{T2} ≈ 90mV), the duty cycle is switched over to 100% and the capacitor C_5 is charged by a current source of I_{ch} − I_{dis}. The external FET is switched off after the cut-off threshold (V_{T5}) is reached. Renewed switching on of the FET is possible only after a power-on reset. The current source, I_{dis}, ensures that the capacitor C_5 is not charged by parasitic currents.

Time delay, td, is as follows: td = C5 ×V_{T5}/ (I_{ch} – I_{dis})

With C_5 = 100 nF and V_{T5} = 10.4 V, I_{ch} =13 μA, I_{dis} = 3 μA,

we have: td = 100 nF ×10.4 V/ (13 μA – 3 μA),

td = 104 ms

2. Current Limitation:

The lamp current is limited by a control amplifier to protect the external power transistor. The voltage drop across an external shunt resistor acts as the measured variable. Current limitation takes place for a voltage drop of V_{T1} ≈ 100 mV. Owing to the difference V_{T1} －V_{T2} ≈10mV, it is ensured that current limitation occurs only when the short-circuit detection circuit has responded.

After a power-on reset, the output is inactive for half an oscillator cycle. During this time, the supply voltage capacitor can be charged so that current limitation is guaranteed in the event of a short-circuit when the IC is switched on for the first time.

Pins 7 and 8, Charge Pump and Output,

Output, Pin 8, is suitable for controlling a power MOSFET. During the active integration phase, the supply current of the operational amplifier is mainly supplied by the capacitor C_3 (bootstrapping). In addition, a trickle charge is generated by an integrated oscillator (f7 ≈ 400 kHz) and a voltage doubler circuit. This permits a gate voltage supply at a duty cycle of 100%

.

Absolute Maximum Ratings

Parameters	Symbol	Value	Unit
Junction temperature	T_j	150	℃
Ambient temperature range	T_{amb}	–40 to +100	℃
Storage temperature range	T_{stg}	–55 to +125	℃

Thermal Resistance

Parameters	Symbol	Value	Unit
Junction ambient	R_{thJA}	120	K/W

Electrical Characteristics

T_{amb} = –40 to +110°C, V_{Batt} = 9 to 16.5 V, (basic function is guaranteed between 6.0 V to 9.0 V) reference point ground, unless otherwise specified (see figure 1). All other values refer to Pin GND (Pin 2).

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Current consumption	Pin 1	I_S			7.9	mA
Supply voltage	Overvoltage detection, stage 1	V_{Batt}			25	V
Stabilized voltage	I_S = 10 mA Pin 1	V_S	24.5		27.5	V
Battery undervoltage detection	– on – off	V_{Batt}	4.4 4.8	5.0 5.4	5.6 6.0	V
Battery overvoltage detection						
Stage 1:	– on – off	V_{Batt}	18.3 16.7	20.0 18.5	21.7 20.3	V
Stage 2: Detection stage 2	– on – off	V_{Batt}	25.5 19.5	28.5 23.0	32.5 26.5	V
Stabilized voltage	I_S = 30 mA Pin 1	V_S	18.5	20.0	21.5	V
Short-circuit protection Pin 6						
Short-circuit current limitation	$V_{T1} = V_S - V_6$	V_{T1}	85	100	120	mV
Short-circuit detection	$V_{T2} = V_S - V_6$	V_{T2}	75	90	105	mV
		$V_{T1} - V_{T2}$	3	10	30	
Delay timer short circuit detection, V_{Batt} =12V Pin 5						
Switched off threshold	$V_{T5} = V_S - V_5$	V_{T5}	10.2	10.4	10.6	V
Charge current		I_{ch}		13		µA
Discharge current		I_{dis}		3		µA
Capacitance current	$I_5 = I_{ch} - I_{dis}$	I_5	5	10	15	mA
Voltage doubler Pin 7						
Voltage	Duty cycle 100%	V_7	$2V_S$			
Oscillator frequency		f_7	280	400	520	kHz
Internal voltage limitation	I_7 = 5 mA (whichever is lower)	V_7	26	27.5	30.0	V
			V_S +14	V_S +15	V_S +16	

Electrical Characteristics （continue）

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Edge steepness	$dV_8/dt = \alpha_4\ dV_4/dt$ dV_8/dt_{max}	α_4	53	63	72 130	V/ms
Gate output	Pin8					
Voltage	Low level	V_8	0.35	0.70	0.95	V
	V_{Batt} = 16.5 V T_{amb} =110℃, R_3=150 Ω				1.5 *)	
	High level, duty cycle 100%			V_7		
Current	V_8 = Low level	I8	1.0			mA
	V_8 = High level, $I_7 > \lvert I_8 \rvert$		- 1.0			
Duty cycle	Min: C_2 = 68 nF Max: V_{Batt} ≤12.4 V V_{Batt} =16.5V, C_2 = 68 nF	t_p/T	15 100 65	18 73	21 81	%
Oscillator						
Frequency	Pin4	f	10		2000	Hz
Threshold cycle Upper	V_8 = High, $\alpha_1 = V_{T100}/V_S$	α_1	0.68	0.7	0.72	
	V_8 =Low, $\alpha_2 = V_{T<100}/V_S$	α_2	0.65	0.67	0.69	
Lower	$\alpha_3 = V_{TL}/V_S$	α_3	0.26	0.28	0.30	
Oscillator current	V_{Batt} = 12 V	$\pm I_{osc}$	34	45	54	μA
Frequency	C_4 open, C_2 = 68 nF duty cycle = 50%	f	56	75	90	Hz

*) Reference point is battery ground

.

Application

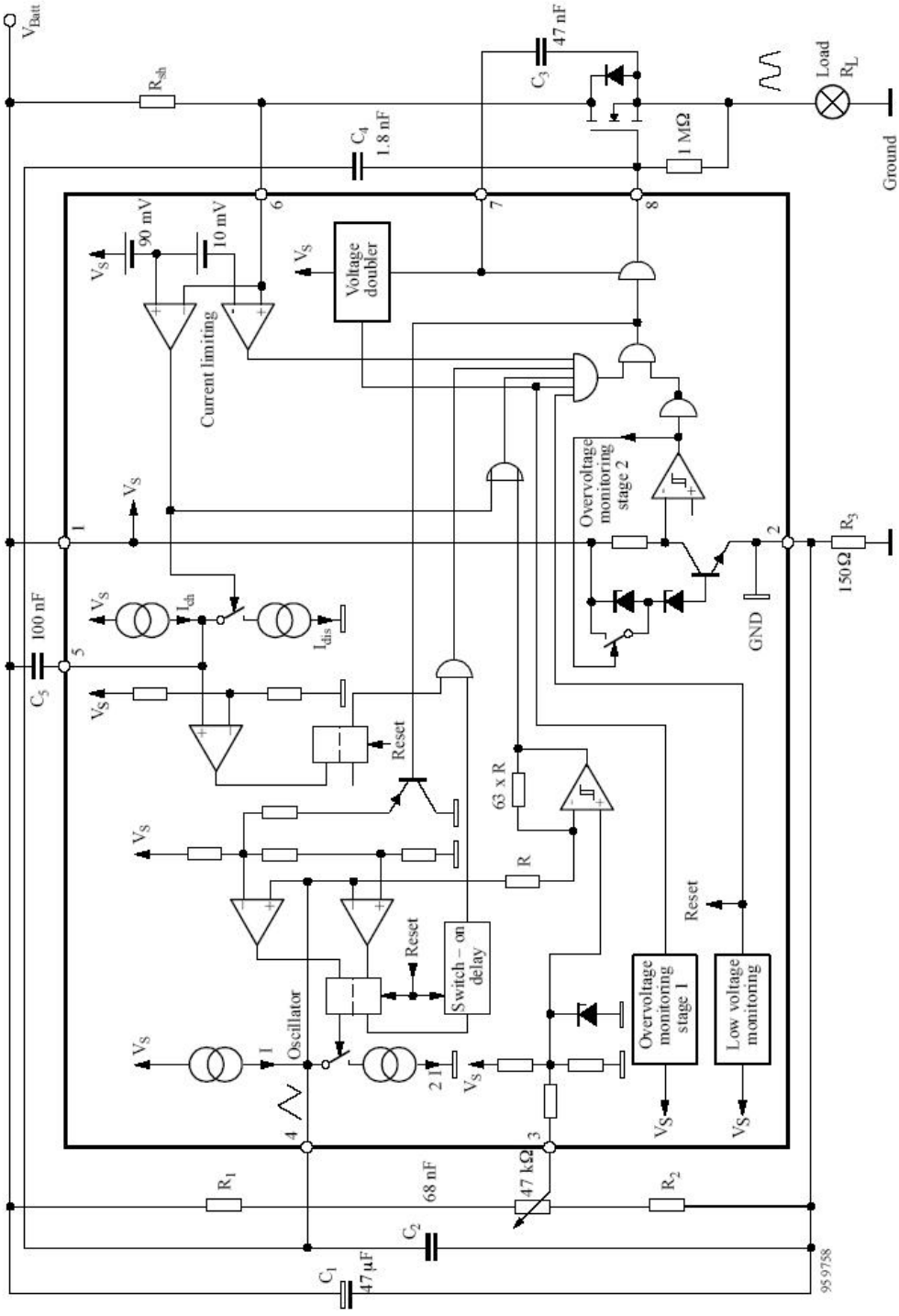
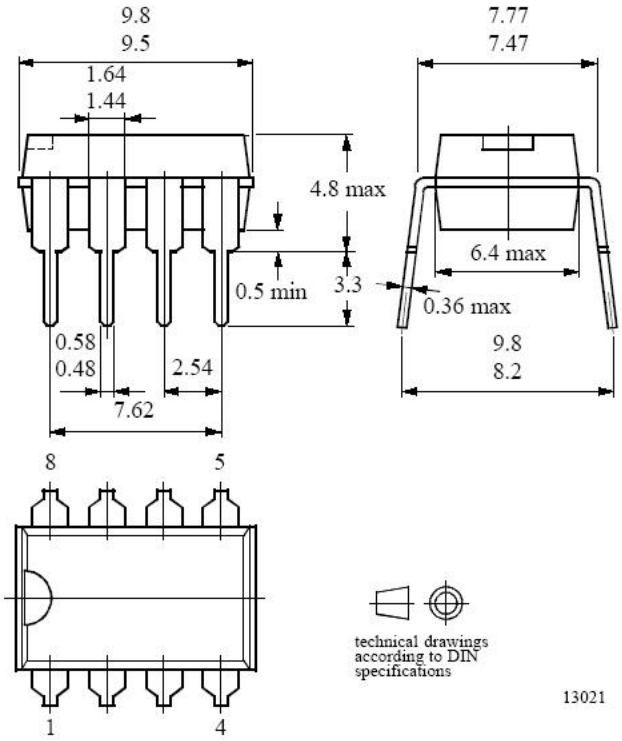


Figure 3. Application Circuitry

Package Information

DIP8

Dimensions in mm



SOP8

Dimensions in mm